WHAT IS CLAIMED IS:

Sub B17

1. An electro-optical device comprising:

at least two transistors provided on an insulating surface;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

2. An electro-optical device comprising:

at least two ~~transistors~~ provided on an insulating surface in a peripheral circuitry of said electro-optical device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

3. An electro-optical device comprising:

at least two transistors provided on an insulating surface in a buffer circuit of a peripheral circuitry of said electro-optical device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

B Cont.

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

4. An electro-optical device comprising:

an active matrix circuit provided on an insulating surface;

at least two transistors provided on said insulating surface in a peripheral circuitry of said electro-optical device provided around said active matrix circuit;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and

B1 cont.

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

5. An electro-optical device comprising: an active matrix circuit provided on an insulating surface;

at least two transistors provided on said insulating surface in a buffer circuit of a peripheral circuitry of said electro-optical device provided around said active matrix circuit;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

B1 Cont.

6. An electro-optical device comprising:

at least two transistors provided on an insulating surface;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline,

wherein said channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

B1 Cont.

7. An electro-optical device comprising: at least two transistors provided on an insulating surface;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline,

wherein said channel-forming regions of said at least two transistors are provided in a common island; and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

8. An electro-optical device comprising:

at least two transistors provided on an insulating surface in a peripheral circuitry of said electro-optical device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

B1 cont.

wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline,

wherein said channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

9. An electro-optical device comprising: at least two transistors provided on an insulating surface in a peripheral circuitry of said electro-optical device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline,

wherein said channel-forming regions of said at least two transistors are provided in a common island; and

B1 Cont.

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

B1 Cont.

10. An electro-optical device which employs a thin-film semiconductor which is formed on an insulating surface, wherein

the thin-film semiconductor has a region which can be regarded as being effectively monocrystalline,

the region contains carbon and nitrogen atoms at a concentration of 5×10^{18} cm^{-3} or less, oxygen atoms at a concentration of 5×10^{19} cm^{-3} or less, and

wherein the region constitutes at least part of a channel-forming region.

Sub D2

11. The device of claim 1 wherein said electro-optical device has a memory.

12. The device of claim 1 wherein said electro-optical device has a decoder.

D

13. The device of claim 1 wherein said electro-optical device is a display system.

14. The device of claim 2 wherein said electro-optical device has a memory.

15. The device of claim 2 wherein said electro-optical device has a decoder.

B

16. The device of claim 2 wherein said electro-optical device is a display system.

17. The device of claim 3 wherein said electro-optical device has a memory.

18. The device of claim 3 wherein said electro-optical device has a decoder.

19. The device of claim 3 wherein said electro-optical device is a display system.

20. The device of claim 4 wherein said electro-optical device has a memory.

21. The device of claim 4 wherein said electro-optical device has a decoder.

22. The device of claim 4 wherein said electro-optical device is a display system.

23. The device of claim 5 wherein said electro-optical device has a memory.

24. The device of claim 5 wherein said electro-optical device has a decoder.

~~25. The device of claim 5 wherein said electro-optical device is a display system.~~

Sub D4

~~26. The device of claim 6 wherein said electro-optical device has a memory.~~

D

~~27. The device of claim 6 wherein said electro-optical device has a decoder.~~

~~28. The device of claim 6 wherein said electro-optical device is a display system.~~

~~29. The device of claim 7 wherein said electro-optical device has a memory.~~

~~30. The device of claim 7 wherein said electro-optical device has a decoder.~~

~~31. The device of claim 7 wherein said electro-optical device is a display system.~~

Sub D5

~~32. The device of claim 8 wherein said electro-optical device has a memory.~~

D

~~33. The device of claim 8 wherein said electro-optical device has a decoder.~~

34. The device of claim 8 wherein said electro-optical device is a display system.

35. The device of claim 9 wherein said electro-optical device has a memory.

C

36. The device of claim 9 wherein said electro-optical device has a decoder.

37. The device of claim 9 wherein said electro-optical device is a display system.

Sub B2

38. The device of claim 1 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

39. The device of claim 1 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

B

40. The device of claim 2 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

41. The device of claim 2 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

42. The device of claim 3 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

43. The device of claim 3 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

B2 Cont.

44. The device of claim 4 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

45. The device of claim 4 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

46. The device of claim 5 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

47. The device of claim 5 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

48. The device of claim 6 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

B2 Cont.

49. The device of claim 6 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

50. The device of claim 7 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

51. The device of claim 7 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

52. The device of claim 8 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

53. The device of claim 8 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

B2 cont.

54. The device of claim 9 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

55. The device of claim 9 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

56. The device of claim 10 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

B2 cont'

57. The device of claim 10 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

add B3>

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